RESPONSE

Claims 1-23 were pending in the Application. Claims 1-23 stand rejected. Claims 1, 17, 18, 19, and 20 are amended by the present amendment. Support for the amendments may be found in the Specification at, for example, page 7, line 23, and page 8, lines 1-3. Applicants submit that no new matter is introduced by the present Amendment. Upon entry of the present Amendment, claims 1-23 will be pending and presented for reconsideration.

Rejections Under 35 U.S.C. §102

Claims 1-20 and 22-23 were rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,457,073 to Barry et al. (hereinafter "Barry").

Rejection of Independent Claim 1 Under 102(e) In View of Barry

Amended claim 1 is directed to a method for transferring portions of a memory block and recites:

(a) configuring a first data mover with a first start address corresponding to a first portion of a source memory block;

(b) configuring a second data mover with a second start address corresponding to a second portion of the source memory block sized differently from the first portion;

(c) verifying that the first portion and the second portion of the course memory block are available for transfer;

(d) after verification, transferring, by the first data mover, the first portion of the source memory block at a first data rate; and

(e) after verification, transferring, by the second data mover, the second portion of the source memory block at a second data rate.

The Office Action suggests that Barry anticipates all of the elements of claim 1. Claim 1 has been amended to further clarify Applicants' invention, and Applicants respectfully traverse

the rejection. Support for the amendments can be found, for example, at least on page 7, lines 14-23 and page 8, lines 1-3. No new matter has been added.

Generally, Barry teaches "the movement of one or more units of data from a source device (either I/O or memory) to a destination device (I/O or memory)." (Col. 5, lines 4-6.) In particular, Barry teaches that "a transfer controller performs data reads and writes from or to system memory or I/O devices." (Col. 6, lines 27-28.) With respect to the transfer, Barry teaches that "[o]nce a transfer has been started there must be some means for the host processor to know when the transfer has completed or reached some 'point of interest'. These 'points of interest' correspond to internal transfer conditions." (Col. 13, lines 6-9.) Barry teaches an internal condition called the "TPC=WAITPC" condition that "is checked during the CHECKPC state 710 of Fig. 7 and causes fetching to pause while the condition is true. (Col. 13, lines 21-23.) Further, "[t]hese conditions ensure that when the transfer controller signals that a transfer is complete, the data is actually valid for a host processor, and data coherence is maintained." (Col. 13, lines 48-50.)

Barry does not teach "verifying that the first portion and the second portion of the course memory block are available for transfer; after verification, transferring, by the first data mover, the first portion of the source memory block at a first data rate; and after verification, transferring, by the second data mover, the second portion of the source memory block at a second data rate." While Barry teaches pausing, in certain situations, "[o]nce a transfer has been started," Barry does not teach verifying that a memory block is available for transfer prior to the beginning of a data transfer. (Col 13, lines 6 and 21-22.) Thus, Barry does not teach or suggest "verifying that the first portion and the second portion of the course memory block are available for transfer" and "after verification, transferring, by the first data mover, the first portion of the source memory block at a first data rate; and after verification, transferring, by the second data mover, the second portion of the source memory block at a second data rate," as recited in amended claim 1.

Since Barry does not teach or suggest this verifying element prior to transferring, Barry does not teach or suggest all of the elements of amended independent claim 1. Thus, Applicants respectfully submit that amended independent claim 1 is patentable in view of Barry. Applicants further submit that claims 2-16, which depend from independent claim 1 and include all of the limitations therein, are also patentable.

Rejection of Independent Claim 17 Under 102(e) In View of Barry

Amended claim 17 is a method for transferring portions of a memory block comprising the steps of:

(a) designating a master data mover;

(b) designating a slave data mover in communication with the master data mover;

(c) transmitting a start address to the master data mover, the start address identifying a first memory portion of a source memory block;

(d) transmitting the start address to the slave data mover to enable the slave data mover to determine a next address, the next address identifying a second memory portion of the source memory block sized differently from the first memory portion;

(e) transmitting a first write address identifying a first memory portion of a target memory block to the master data mover and a second write address identifying a second memory portion sized differently than the first memory portion of the target memory block to the slave data mover;

(f) verifying that the first portion and the second portion of the source memory block are available for transfer;

(g) after verification, transferring the first memory portion of the source memory block to the first write address identifying the first memory portion of the target memory block at a first data rate; and

(h) after verification, transferring the second memory portion of the source memory block to the second write address identifying the second memory portion of the target memory block at a second data rate.

The Office Action suggests that Barry anticipates all of the elements of claim 17. Claim 17 has been amended to further clarify Applicants' invention, and Applicants respectfully traverse the rejection. Support for the amendments can be found, for example, at least on page 7, lines 14-23 and page 8, lines 1-3. No new matter has been added.

As discussed above with respect to claim 1, Barry does not teach or suggest "verifying that the first portion and the second portion of the source memory block are available for transfer; after verification, transferring the first memory portion of the source memory block to the first write address identifying the first memory portion of the target memory block at a first data rate; and after verification, transferring the second memory portion of the source memory block to the second write address identifying the second memory portion of the target memory block at a second data rate." In particular, Barry does not teach or suggest transferring a memory portion after verifying that the memory portion is available for transfer. Thus, Barry does not teach or suggest all of the recited elements of amended claim 17. Accordingly, Applicants respectfully submit that independent claim 17 is patentable over Barry. Applicants further submit that claims 18-19, which depend from independent claim 17 and incorporate all of the limitations therein, are also patentable over Barry.

Rejection of Independent Claim 20 Under 102(e) In View of Barry

Amended claim 20 is directed to a system to transfer portions of a memory block and recites:

(a) a first data mover;

(b) a second data mover in communication with the first data mover over a DM communications bus;

(c) a first memory component having a first portion and a second portion sized differently from the first portion and in communication with the first data mover and the second data mover over a first DM-memory bus; and

(f) a second memory component in communication with the first data mover and

the second data mover over a second DM-memory bus,

(e) a boundary window to ensure that the first and second memory components are available for transfer, wherein the first data mover and the second data mover check the boundary window before transferring at least one of the first memory portion and the second memory portion;

wherein the first data mover transfers the first memory portion to the second memory component over the first DM-memory bus at a first data transfer rate after checking the boundary window, and

wherein the second data mover transfers the second memory portion to the second memory component over the second DM-memory bus at a second data transfer rate after checking the boundary window.

The Office Action suggests that Barry anticipates all of the elements of claim 20. Claim 20 has been amended to further clarify Applicants' invention, and Applicants respectfully traverse the rejection. Support for the amendments can be found, for example, at least on page 7, lines 14-23 and page 8, lines 1-3. No new matter has been added.

As discussed above with respect to claim 1, Barry does not teach or suggest ensuring that a memory block is available for transfer, i.e., Barry does not teach or suggest "a boundary window to ensure that the first and second memory components are available for transfer, wherein the first data mover and the second data mover check the boundary window before transferring at least one of the first memory portion and the second memory portion; wherein the first data mover transfers the first memory portion to the second memory component over the first DM-memory bus at a first data transfer rate after checking the boundary window, and wherein the second data mover transfers the second memory portion to the second memory component over the second DM-memory bus at a second data transfer rate after checking the boundary window." In particular, Barry does not teach or suggest transferring a memory portion after verifying that the memory portion is available for transfer.

Thus, Barry does not teach or suggest all of the recited elements of amended claim 20. Accordingly, Applicants respectfully submit that independent claim 20 is patentable over Barry. Applicants further submit that claims 21-23, which depend from independent claim 20 and incorporate all of the limitations therein, are also patentable over Barry.

Priem Fails to Cure the Deficiencies of Barry

Claim 21 is rejected under 35 U.S.C. §103(a) as being unpatentable over Barry in view of U.S. Patent No. 6,065,071 to Priem et al. (hereinafter "Priem"). Applicants respectfully traverse the rejection.

Generally, Priem teaches "accomplishing faster writes of data directly from an application program to I/O devices while providing means for hand[l]ing unimplemented operations in input/output devices which include first-in first-out (FIFO) buffers." (Col. 2, lines 19-22.) In particular, Priem teaches where the "application program executing on the central processor may directly read and write to the hardware of the input/output control unit." (Col. 4, lines 44-47.) Furthermore, Priem teaches "[i]f the command requires that data be transferred to or from the application, the input/output device performs the transfer using the DMA unit 35." (Col. 6, lines 23-25.)

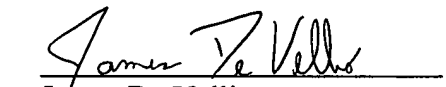
Priem does not, however, teach or suggest verifying that the first portion and the second portion of the source memory block are available for transfer and transferring the memory block(s) after verification, as recited in claims 1 and 17. Moreover, Priem also does not teach or suggest the use of a blocked boundary window to ensure that the first and second memory components are available for transfer prior to data transfer, as recited in claim 20.

Thus, Priem and Barry, alone or in combination, fail to teach or suggest all of the elements of amended independent claims 1, 17, and 20. Accordingly, Applicants submit that these claims are patentable over Barry and Priem. Additionally, since claims 2-16, 18-19, and 21-23 depend from independent claims 1, 17, and 20, respectively, Applicants submit that these claims are also patentable.

CONCLUSION

Claims 1-23 were pending in the Application. Claims 1-23 stand rejected. Claims 1, 17, 18, 19, and 20 are amended by the present Amendment. Applicants request that the Examiner reconsider the application and claims 1-23 in light of the foregoing Amendment and Response, and respectfully submit that the claims, as amended, are in condition for allowance. If, in the Examiner's opinion, a telephonic interview would expedite the favorable prosecution of the present application, the undersigned attorney would welcome the opportunity to discuss any outstanding issues, and to work with the Examiner toward placing the application in condition for allowance.

Regards,



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